



正基科技股份有限公司

SPECIFICATION

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正基科技股份有限公司



AC5035M2

Data Sheet

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1. Introduction

1.1 Overview

The AMPAK Technology® APM5035M2 module is a multipurpose 3GPP Release 17 Redcap module. It was envisioned to operate in conjunction with a host board that must provide power and control for its various applications. The module chipset is Qualcomm SDX35, which supports 4G and 5G technologies and was designed with an advanced 4 nm process for superior performance and power efficiency.

1.2 Block Diagram

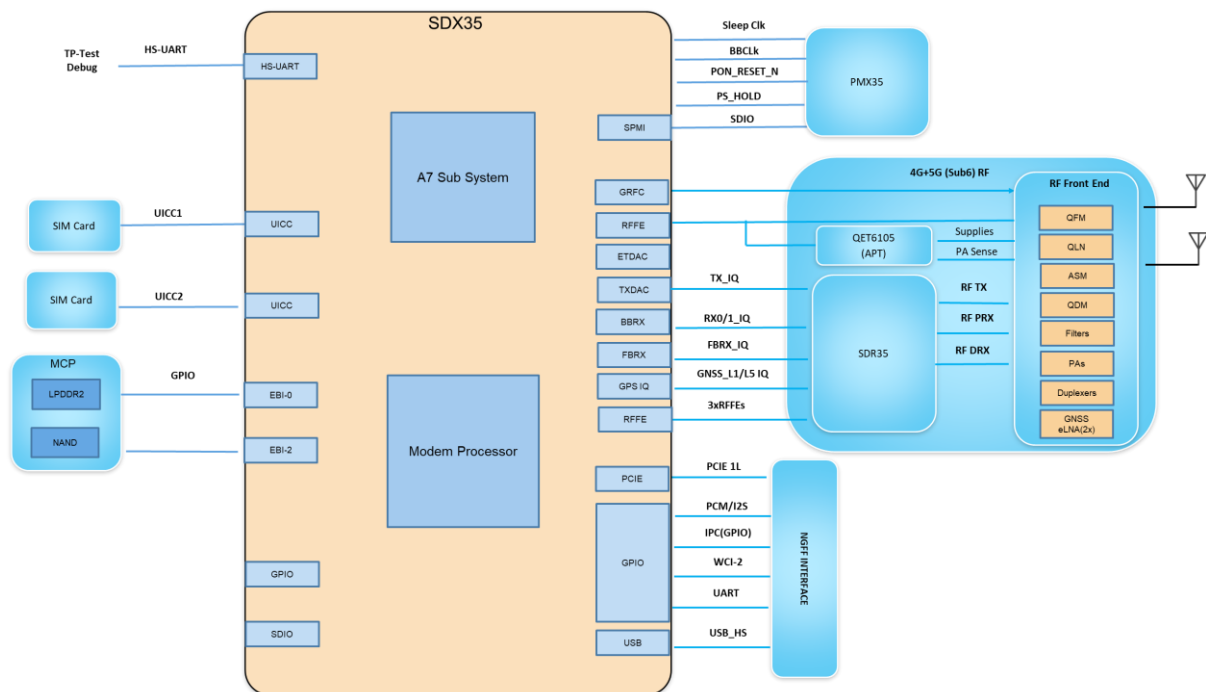


Figure 1-1 High-level block diagram

2. General Specification

2.1 Features

Table 2-1 Module features

Feature	AC5035M2 module
Processors	
Applications	Arm Cortex A7 processor at up to 1.7 GHz
Modem system	Qualcomm DSP Q6 always on subsystem
Always-on subsystem	Cortex-M3 up to 200 MHz
Memory and storage support	
Memory	2Gb LPDDR2 at 533MHz
Storage	4Gb NAND flash
Connectivity	
UIM	Two UIM interfaces
USB	One: HS USB 2.0
PCIe	One: GEN 2.0, 1 lane
Audio Interfaces	Primary and secondary I2C and PCM
RF support	
Standard compliance	3GPP Release 17 Red. Cap. 5G NR sub-6
Multimode support	3GPP LTE FDD and TDD 5G NR sub-6 GHz
Supported bands	See Table xxx
Antenna Ports	2x WWAN (include GNSS)
Technology frequency range	4G, 5G NR sub-6, 600 MHz to 5.0 GHz
Maximum bandwidth	20 MHz
SRS	1T/2R (TDD_LTE)
GNSS	GPS, GLONASS, Galileo, and BeiDou support GNSS path L1
Operation mode	Standalone mode (SA) (5G), No CA support (4G/5G)
MIMO support (4G/5G sub-6)	2 x 2 MIMO

Power tracking	APT
Module chips	
Modem	SDX35
Memory and Storage	JSFCBA3YH3BBG-425A MCP
eSIM(optional)	MFXS-M006b-MFOCMW
Transceiver	SDR125
RF front end	QPA6590, QFM6515, QPM6579, QDM5302
Envelop tracker	1x QET6105
PMIC primary	PMX35
38.4 MHz crystal	EXS00A-CS12755
Power supply	
Single rail	3.3 V from the host
Data Rate	
Speed	Uplink : 50-100 Mbps , Downlink: 180 -220 Mbps
Mechanical/thermal	
XY-dimension	30 mm x 42 mm
Z-dimension	1.67 mm per M.2 specification
PCB thickness	0.8 mm \pm 10% per M.2 specification
Mounting	Single sided (when debug is not included)
Shielding	Two-piece metal shield 1.35 mm in height
Functional temperature[°C]	-30 to +75
Extended temperature[°C]	-40 to +85
Performance	-20 to +60

2.2

Form factor

The AC5035M2 module is manufactured on a type 3042 standard add-in card with the following main characteristics:

- Dimensions: 30 mm x 42 mm
- Dimensions tolerances: \pm 0.15mm

- Socket family: socket 2
- Notch: key B
- Number of pins: 75
- Mounting: single-sided



Figure 2-1 AC5035M2 module form factor

2.3 Pin Definition

The AC5035M2 module is available in dual-sided 75-pin key-B type connector. The keying scheme and the pinout diagram are shown in the following figure. For more information on module-specific pin characteristics.

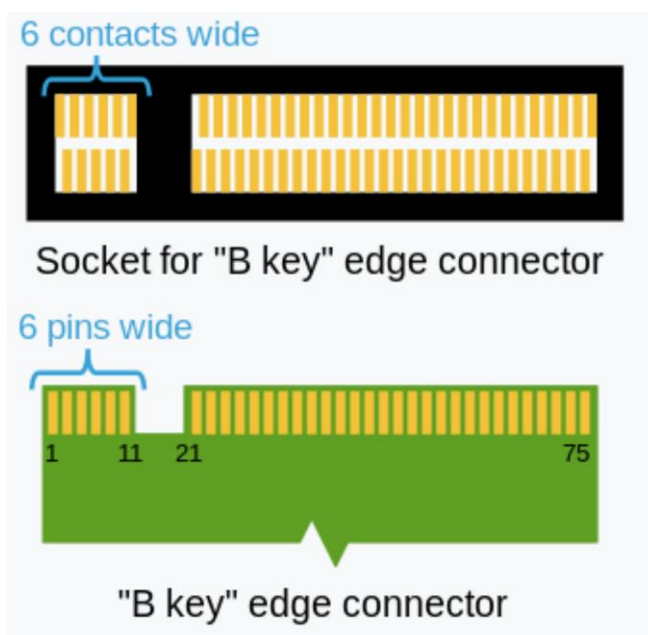


Figure 2-2 Dual-sided key-B PCIe connector pinout

2.4 I/O parameter definitions

Table 2-2 I/O parameter definitions

Pin attribute	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
OD	Open drain
PU	Pull-up
PD	Pull-down

2.5 Pin Description

Table 2-3 Pin description

Pin no.	Pin name	Pin characteristic		Module specific functional description
		Voltage	Type	
1	CONFIG_3	0/NC	DO	Indicates the configuration of the Add-in card
2	3.3 V	3.3	PI	Power supply input
3	GND	0/1.8	DI	Defines the module communication interface Low: PCIe (default) High: USB
4	3.3 V	3.3	PI	Power supply input
5	GND	0	PI	Return path current
6	FULL_CARD_POWER_OF F#	0/1.8/3.3	DI/PD	A single control to turn off the module. Active Low
7	USB_D+	0/3.3	DI/DO	USB Data+ defined in the USB 2.0 Specification
8	W_DISABLE1#	0/1.8/3.3	DI/PU	Disable radio operation Active low
9	USB_D-	0/3.3	DI/DO	USB Data- defined in the USB 2.0 Specification
10	GPIO_9/LED_1#/IPC_	0/3.3	DO/OD	Indicate LED status

	7			Open drain and active low
11	GND	0	PI	Return path current
12	ADD-IN CARD KEY B	Notch location		
13	ADD-IN CARD KEY B	Notch location		
14	ADD-IN CARD KEY B	Notch location		
15	ADD-IN CARD KEY B	Notch location		
16	ADD-IN CARD KEY B	Notch location		
17	ADD-IN CARD KEY B	Notch location		
18	ADD-IN CARD KEY B	Notch location		
19	ADD-IN CARD KEY B	Notch location		
20	GPIO_5/AUDIO_0/RFU	0/1.8	DI/DO	Primary I2S serial clock
21	CONFIG_0	0/NC	DO	Indicate the configuration of the Add-in card
22	GPIO_6/AUDIO_1/RFU	0/1.8	DI	Primary I2S data0 signal or UART debug receiver (Rx)
23	GPIO_11-WoWWAN#	0/1.8	OD/DI	Wake the host by the WWAN device. Active low
24	GPIO_7/AUDIO_2/RFU / IPC_5	0/1.8	PO	1.8 V power supply for MIPI antenna tuner or Primary I2S data1 signal
			DO	
25	DPR	0/1.8	DI	BodySAR detection pin
				When high: Disable the SAR power back off
				When low: Enable the SAR power back off
26	GPIO_10/W_DISABLE_2#	0/1.8/3.3	DI/PU	Disable GPS operation. Active low
27	GND	0	PI	Return path current
28	GPIO_8/AUDIO_3/RFU / IPC_6	0/1.8	DI/DO	Primary I2S word select or UART debug transmitter (Tx)
29	NC			NOTE It is NC in the M.2 design
30	UIM-RESET	0/1.8/2.85	DO	UIM1 reset signal
31	NC			NOTE It is NC in the M.2 design

32	UIM-CLK	0/1.8/2.85	DO	UIM1 clock reference signal
33	GND	0	PI	Return path current
34	UIM-DATA	0/1.8/2.85	DI/DO/PU	UIM1 data signal
35	NC			NOTE It is NC in the M.2 design
36	UIM-PWR	0/1.8/2.85	PO	UIM1 power supply
37	NC			NOTE It is NC in the M.2 design
38	NC	0/1.8	DI	Wi-Fi co-existence with n79 GPIO control (WLAN to SDR)
39	GND	0	PI	Return path current
40	GPIO_0/GNSS_SCL/ SIM_DET2/IPC_0	0/1.8	DI/PU	An indication to the modem to detect SIM2 insertion/removal
41	PETn0	0/1.2	DO	PCIe data transmitter (Tx0) differential pair – negative
42	GPIO_1/GNSS_SDA/ UIM_DATA2/IPC_1	0/1.8/2.85	DI/DO	UIM2 data signal
43	PETp0	0/1.2	DO	PCIe data transmitter (Tx0) differential pair – positive
44	GPIO_2/GNSS_IRQ/ UIM_CLK2/IPC_2	0/1.8/2.85	DO	UIM2 clock reference signal
45	GND	0	PI	Return path current
46	GPIO_3/SYSCLK/ GNSS_0/UIM_RST2/ IPC_3	0/1.8/2.85	DO	UIM2 reset signal
47	PERn0	0/1.2	DI	PCIe data receiver (Rx0) differential pair – negative
48	GPIO_4/TX_BLANKING / GNSS_1/UIM_PWR2/ IPC_4	0/1.8/2.85	PO	UIM2 power supply
49	PERp0	0/1.2	DI	PCIe data receiver (Rx0) differential pair – positive
50	PERST#	0/3.3	DI	Functional reset to the module. Active low. Defined in the PCIe CEM Specification
51	GND	0	PI	Return path current

52	CLKREQ#	0/3.3	OD	Reference clock request signal. Active low. Defined in the PCIe CEM Specification
53	REFCLKn	0/0.7	DI/DO	PCIe reference clock- signal (100 MHz). Defined in the PCIe CEM Specification
54	PEWAKE#	0/3.3	OD	Request the system to return from a sleep/suspended state. Active low. Defined in the PCIe CEM specification
55	REFCLKp	0/0.7	DI/DO	PCIe reference clock+ signal (100 MHz). Defined in the PCIe CEM specification
56	NC(RFFE_DATA)	0/1.8	DO	MIPI data for external tunable antenna
57	GND	0	PI	Return path current
58	NC(RFFE_CLK)	0/1.8	DO	MIPI clock for external tunable antenna
59	NC			It is NC in the M.2 design
60	COEX3	0/1.8	DO	Wi-Fi co-existence with n79 GPIO control (WLAN to SDR) QPM6579 FBRX_OUT
61	NC			It is NC in the M.2 design
62	COEX_RXD	0/1.8	DI	For LTE/WLAN co-existence. LTE_FRAME_SYNC
63	NC			It is NC in the M.2 design
64	COEX_TXD	0/1.8	DO	For LTE/WLAN co-existence. LTE_ACTIVE
65	NC			It is NC in the M.2 design
66	SIMDETECT	0/1.8	DI/PU	An indication to the modem to detect SIM1 insertion/removal
67	RESET#	0/1.8	DI/PU	Reset the WWAN solution. Active low
68	SUSCLK(GNSS_0)	0/1.8	DO	NAV_GPIO_1_DR_SYNC
69	CONFIG_1	0/NC	DO	Indicate the configuration of the Add-in card
70	3.3 V	3.3	PI	Power supply input
71	GND	0	PI	Return path current

72	3.3 V	3.3	PI	Power supply input
73	GND(VIO_CFG)	0/NC	PI	Indicate an independent IO voltage domain for sideband signals
				VIO_CFG = NC for 1.8 V IO VIO_CFG = GND for 3.3 V IO
74	3.3 V	3.3	PI	Power supply input
75	CONFIG_2	0/NC	DO	Indicate the configuration of the Add-in card

3. Electronics Specification

3.1 Absolute maximums

No functionality is guaranteed outside the following operating specifications.

Table 3-1 Absolute maximum ratings

Symbol	Pin number	Parameter	Conditions	Min	Max	Unit
3.3 V	2, 4, 70, 72, 74	Supply voltage	–	3.135	3.465	V
		Ripple voltage	1 Hz to 100 kHz	–	100	mVpp
		Current consumption limit (max avg at 100 μ s)	–	–	2500	mA

NOTE Transmitter burst activity must also be accounted for in the 100 mVpp ripple limit

3.2 Logic signals

The 3.3 V and 1.8 V module logic levels specifications for single-ended digital signals are given in the following tables.

Table 3-2 DC specification for 3.3 V logic signaling

Symbol	Parameter	Condition	Min	Max	Unit
3.3V	Supply voltage	–	3.135	3.465	V
V_{IH}	Input high voltage	–	2.0	3.6	V
V_{IL}	Input low voltage	–	-0.5	0.8	V
I_{OL}	Output low current for open-drain signals	0.4 V	4	–	mA
I_{OH}	Output high current for open-drain signals	0.4 V	9	–	mA
I_{IN}	Input leakage current	0 V to 3.3 V	-10	+10	μ A
I_{LKG}	Output leakage current	0 V to 3.3 V	-50	+50	μ A

Table 3-3 DC specification for 1.8 V logic signaling

Symbol	Parameter	Condition	Min	Max	Unit
VDD18	Supply voltage	–	1.7	1.9	V
V_{IH}	Input high voltage	–	0.7 * VDD18	VDD18 + 0.3	V
V_{IL}	Input low voltage	–	-0.3	0.3 * VDD18	V
V_{OH}	Output high voltage	0.4 V	VDD18 + 0.45	–	V
V_{OL}	Output low voltage	0.4 V	–	0.45	V

I_{IN}	Input leakage current	0 V to VDD18	-10	+10	μA
I_{LKG}	Output leakage current	0 V to VDD18	-50	+50	μA

NOTE For more detailed information on PCIe electrical requirements, logic signaling specifications, and other electrical features, see *PCI Express M.2 Specification Revision 4.0, Version 1.0*.

4. Application interfaces

4.1 Peripheral components interface express (PCIe)

PCIe communication between the module and the host is supported either via one lane on Gen 4 or via two lanes on Gen 3. The interface is also backward compatible with the PCIe Gen 2.

Table 4-1 PCIe bus interface pins

Pin number	Pin name	Pin attribute	Functional description
53	REFCLKn	DI/DO	PCIe reference clock signal (100 MHz) differential pair – negative
55	REFCLKp	DI/DO	PCIe reference clock signal (100 MHz) differential pair – positive
54	PEWAKE#	OD	PCIe WAKE#. Open drain with pull-up on the module. Active low
52	CLKREQ#	OD	Reference clock request signal. Open Drain with pull up on module. Active low.
50	PERST#	DI	PCIe functional reset
49	PERp0	DI	PCIe data receiver (Tx0) differential pair – positive
47	PERn0	DI	PCIe data receiver (Tx0) differential pair – negative
43	PETp0	DO	PCIe data transmitter (Rx0) differential pair – positive
41	PETn0	DO	PCIe data transmitter (Rx0) differential pair – negative
37	PERp1 (NC in the design)	DI	PCIe data receiver (Tx1) differential pair – positive
35	PERn1 (NC in the design)	DI	PCIe data receiver (Tx1) differential pair – negative
31	PETp1 (NC in the design)	DO	PCIe data transmitter (Rx1) differential pair – positive
29	PETn1 (NC in the design)	DO	PCIe data transmitter (Rx1) differential pair – negative

NOTE The AC coupling capacitors required for the PCIe (Tx) signals are featured on the module while those required for PCIe (Rx) signals must be included in the host.

4.2 Universal serial bus (USB)

The legacy USB 2.0 is available in the module.

Table 4-2 USB interface pins

Pin no.	Pin name	Functional description
7	USB_D+	HS USB 2.0 data transmitter/receiver differential pair – positive
9	USB_D-	HS USB 2.0 data transmitter/receiver differential pair – negative

4.3 User identity module (UIM)

The UIM interface is compliant with ETSI and IMT-2020 standards and supports both Class B (3.0 V ± 10%) and Class C (1.8 V ± 10%) SIM cards. Two separate UIM interfaces are available in the module, namely UIM1 and UIM2, and they can both be used simultaneously. Either the user can have two external SIM cards or one external SIM and one internal (eSIM optional). When the internal eSIM is used, only the UIM1 interface will be available externally.

Table 4-3 UIM1 and UIM2 interface pins

Pin number	Pin name	Pin attribute	Functional description
30	UIM_RESET	DO	SIM Card 1 reset signal Active low
32	UIM_DATA	DI/DO/PU	SIM Card 1 bi-directional data signal
34	UIM_CLK	DO	SIM Card 1 reference clock signal
36	UIM_PWR	PO	SIM Card 1 power supply (provided by the module to the host)
66	SIMDETECT	PU	SIM Card 1 presence indication signal
46	GPIO_3/SYSCLK/GNSS_0/ UIM_RST2/IPC_3	DO	SIM Card 2 reset signal Active low
42	GPIO_1/GNSS_SDA/UIM_DATA2/ IPC_1	DI/DO/PU	SIM Card 2 bi-directional data signal
44	GPIO_2/GNSS_IRQ/UIM_CLK2/ IPC_2	DO	SIM Card 2 reference clock signal

48	GPIO_4/TX_BLANKING/GNSS_1/ UIM_PWR2/IPC_4	PO	SIM Card 2 power supply (provided by the module to the host)
40	GPIO_0/GNSS_SCL/SIM_DET2/ IPC_0	PU	SIM Card 2 presence indication signal
3, 5, 11, 27, 33, 39, 45, 51, 57, 71	GND		UIM1 and UIM2 reference ground common to module ground

5. Control pins and status indicators

The following table summarizes the control signals and the status indicators featured in the module.

Table 5-1 Control signals and status indicators

Pin number	Pin name	Pin attribute	Functional description
6	FULL_CARD_POWER_OFF#	DI/PD	Turns the module ON/OFF
8	W_DISABLE1#	DI/PU	Enables/disables the radio operation
26	GPIO_10/W_DISABLE2#	DI/PU	Enables/disables the GPS/GLONASS operation (option, default no)
10	GPIO_9/LED_1#/IPC_7	OD/DO	Indicates if the RFFE is ON or OFF
23	GPIO_11-WoWWAN#	OD/DO	Wakes up the host
25	DPR	DI/PU	Enables/disables SAR power back off
67	RESET#	PU	Resets the module

5.1 FULL_CARD_POWER_OFF#

The FULL_CARD_POWER_OFF# (FCPO#) is the module's hard reset, which is made available externally through pin 6. The input pin features an internal 100 kΩ pull-down resistor and can be driven either by 3.3 V or 1.8 V signals.

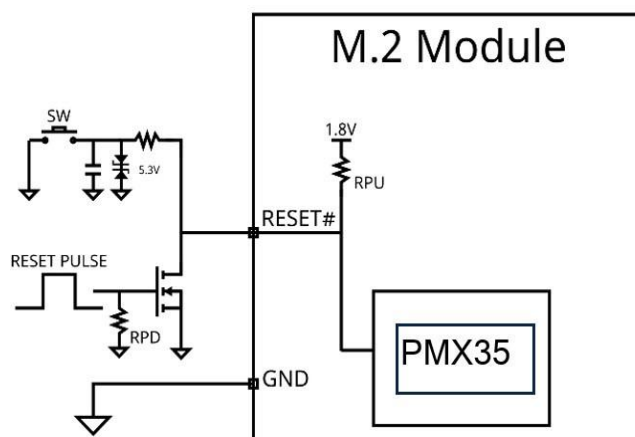


Figure 5-1 FULL_CARD_POWER_OFF circuit diagram

Table 5-2 FULL_CARD_POWER_OFF# status description

Logic level	Module status	Status description
Low (0 V)	OFF	SDX35 M.2 module is OFF
High (1.8 V/3.3 V)	ON	SDX35 M.2 module is ON

5.2 RESET#

The RESET# is a 1.8 V active low signal that when asserted takes the module immediately to the reset condition. The input pin features an internal 100 kΩ pull-up resistor to a 1.8 V internal supply. As shown in the following figure, the reset pulse signal can be either sent through an external GPIO or through a discrete push-button for manual use.

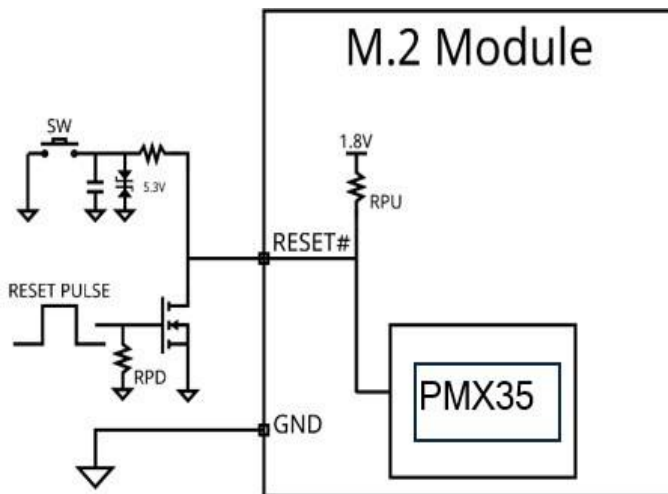


Figure 5-2 RESET# circuit diagram

Be aware that when the RESET# signal is triggered the modem is disconnected from the network, the system drivers are removed, and all data in the module is lost.

Table 5-3 RESET# status description

Logic level	Module status	Status description
Low (0 V)	Reset	The module enters in reset mode and only boots when the signal is high again
High (1.8 V)	ON	The module is ON

5.3 W_DISABLE# and W_DISABLE2#

W_DISABLE1# and W_DISABLE2# are two low-active input pins that are made available externally for enabling/disabling the radio and the GPS/GLONASS operation. Both pins feature an internal pull-up resistor that should be configured using software to either a 3.3 V or 1.8 V rail, depending on the host. Both voltage rails are supported by the PMX35 GPIO.

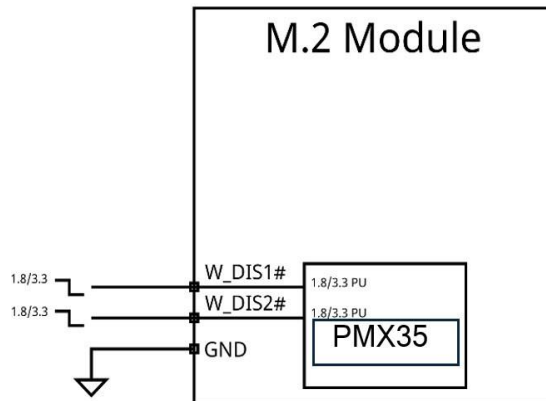


Figure 5-3 W_DISABLE1# and W_DISABLE2# circuit diagram

Table 5-4 W_DISABLE1# status description

Logic level	Module status	Status description
W_DISABLE1#		
Low (0 V)	Radio OFF	WWAN is disabled, no RF operation is allowed
High (1.8 V/3.3 V)	Radio ON	WWAN is enabled, RF operation allowed (requires internal pull-up via software)
W_DISABLE1#		
Low (0 V)	GPS/GLONASS ON	GPS/GLONASS is disabled, no RF operation is allowed
High (1.8 V/3.3 V)	GPS/GLONASS OFF	GPS/GLOBASS is enabled, RF operation is allowed (requires internal via using software)

5.4 LED_1#

The LED_1# output pin is internally connected to 10 mA sink current GPIO and must be used to drive an external LED, indicating the radio status of the module. As depicted in the following figure, a current-limiting resistor must be placed in series with the external LED to reduce the power consumption.

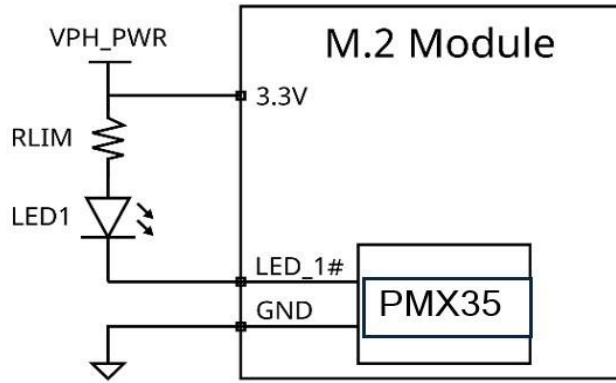


Figure 5-4 LED_1# reference circuit diagram

Table 5-5 LED_1# status description

Logic level	LED status	Status description
Low (0 V)	ON	Radio is not capable of transmitting and the LED is emitting light
High (3.3 V)	OFF	Radio can transmit and the LED is not emitting light

5.5 WoWWAN#

The WoWWAN# open-drain output pin is used to send a wake-up signal from the module to the host. This signal is a one-second-long low-level pulse and for this reason requires a pull-up resistor on the host board.

Table 5-6 WoWWAN# status description

Logic level	Host status	Status description
1 sec-long Low (0 V)	Wake-up	Data is incoming and the module wakes up the host
High (3.3 V)	Idle/sleep	The host is waiting for a wake-up signal from the module

5.6 DPR

The dynamic power reduction (DPR) input pin is used by wireless devices to meet regulatory specific absorption rate (SAR) requirements for RF exposure. The signal must be provided by the host sensor as a response to the proximity of the wireless device, triggering a power reduction in the module's radio transmission. The power reduction required varies depending on the application and must be ultimately determined by the OEM and card vendor. The maximum Tx power can be set by AT commands when the DPR pin is low.

Table 5-7 DPR status description

Logic level	Module status	Status description
Low (0 V)	SAR enabled	Radio is capable of transmitting
High (1.8 V)	SAR disabled	Radio is not capable of transmitting

6. Configuration pins

In addition to the control pins, the module provides four other pins to determine the specific configuration of M.2 add-in card and indicate whether the card is present or not. The following table shows the internal connections of module configuration pins. To understand the meaning of each of the 16 possible decodes, see *PCI Express M.2 Specification Rev 4.0*.

Table 6-1 CONFIG[3..0] pin configuration

CONFIG_0 (Pin# 21)	CONFIG_1 (Pin# 69)	CONFIG_2 (Pin# 75)	CONFIG_3 (Pin# 1)
Open	Ground	Ground	Open

The host must provide a pull-up resistor for each of these pins to either 1.8 V or 3.3 V .

7. RF support

The following figure presents the RF high-level block diagram of the module, including its transceiver, three antennas, low noise amplifiers (LNA), power amplifiers (PA), filters, envelop trackers, and all its main connections.

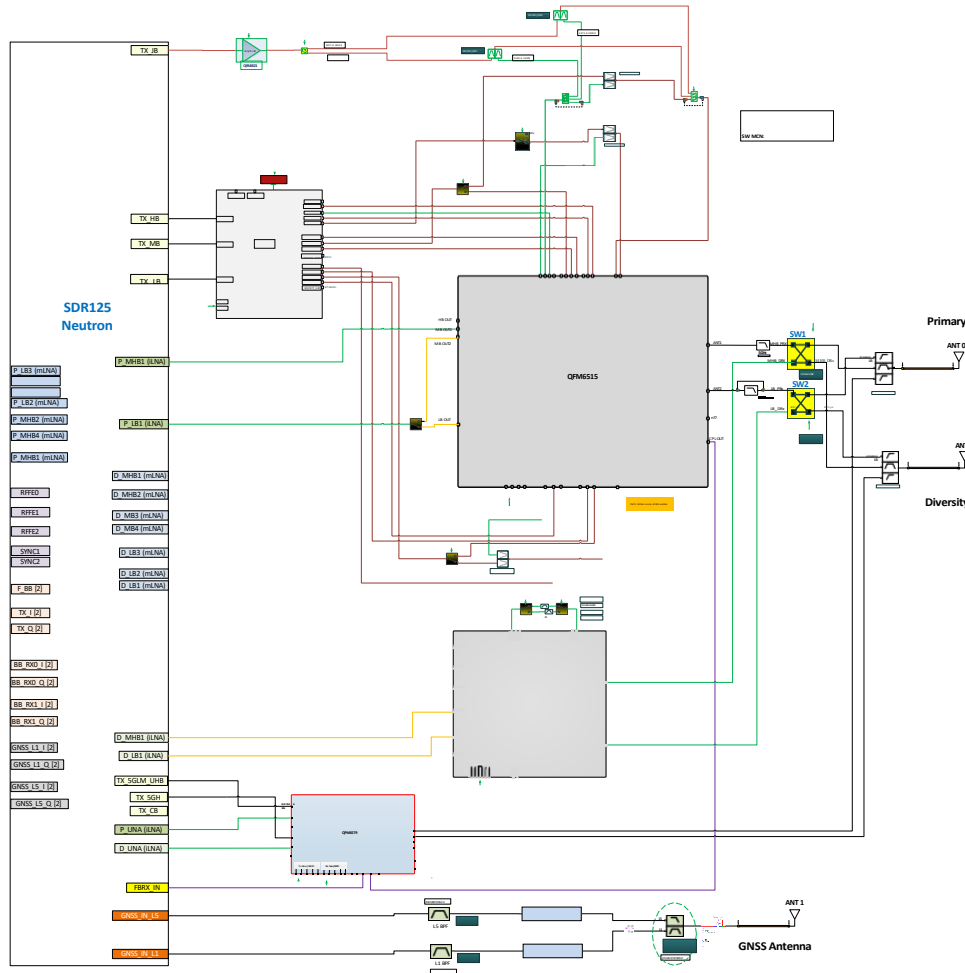


Figure 7-1 AC5035M2 module RF high-level block diagram

The frequency range of each antenna supported band group is listed in the following table according to their block diagram colors. For information on location of antennas, see [Mechanical information](#).

Table 7-1 Band group frequencies of antennas

Port	Band group	Frequency range (MHz)
ANT1	LB TRX0	617 – 960
	MHB TRX0	1695 – 2690
	N77/N78/N79 TRX0	3300 – 5000
ANT4	LBRX1	617 – 960
	MHBRX1	1695 – 2690

	N77/N78/N79 RX1/SRS TX	3300 – 5000
ANT2 (option, default no)	GNSS L1/L5	1164 – 1610

Table 7-2 Supported RF bands

Technology	Supported bands
LTE	TDD: 34, 38, 39, 40, 41, 42, 43, 48 FDD: 1, 2, 3, 4, 5, 7, 8, 12, 13, 14, 17, 18, 19, 20, 21, 25, 26, 28, 30, 66, 70, 71
5G NR	n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n30, n38, n40, n41, n48, n66, n70, n71, n77, n78, n79

8. Mechanical Information

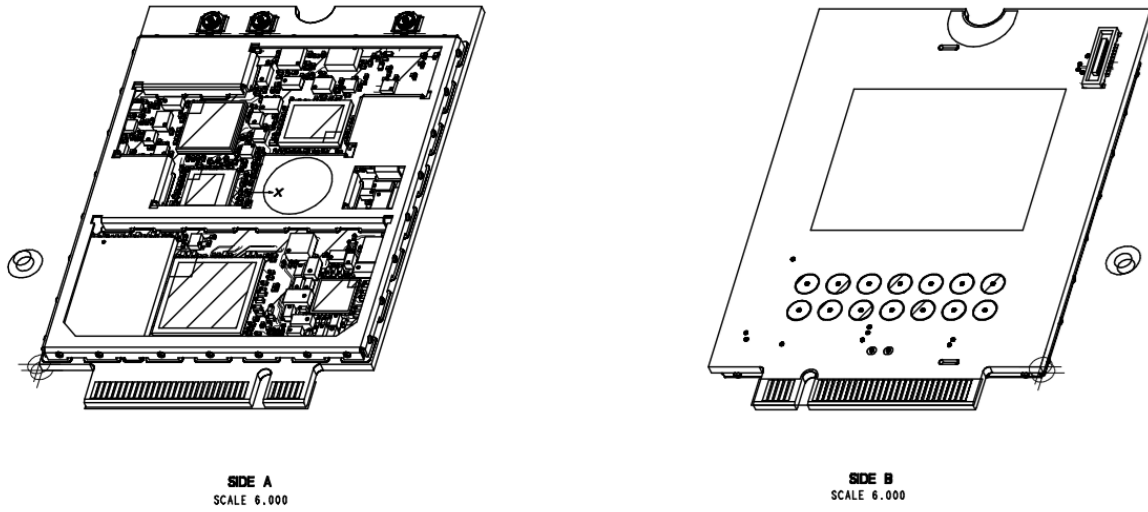


Figure 8-1 Module 3D overview

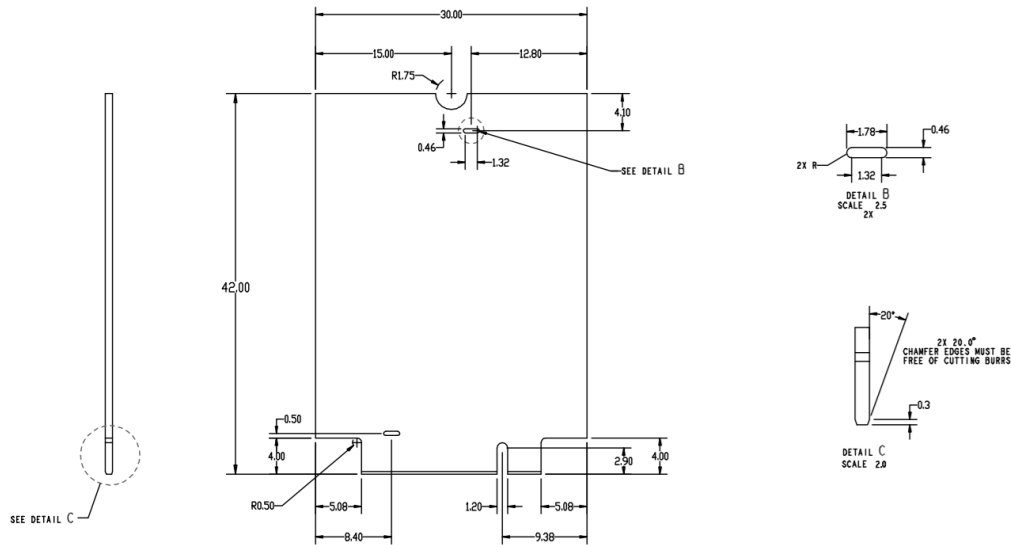


Figure 8-2 Physical Dimension

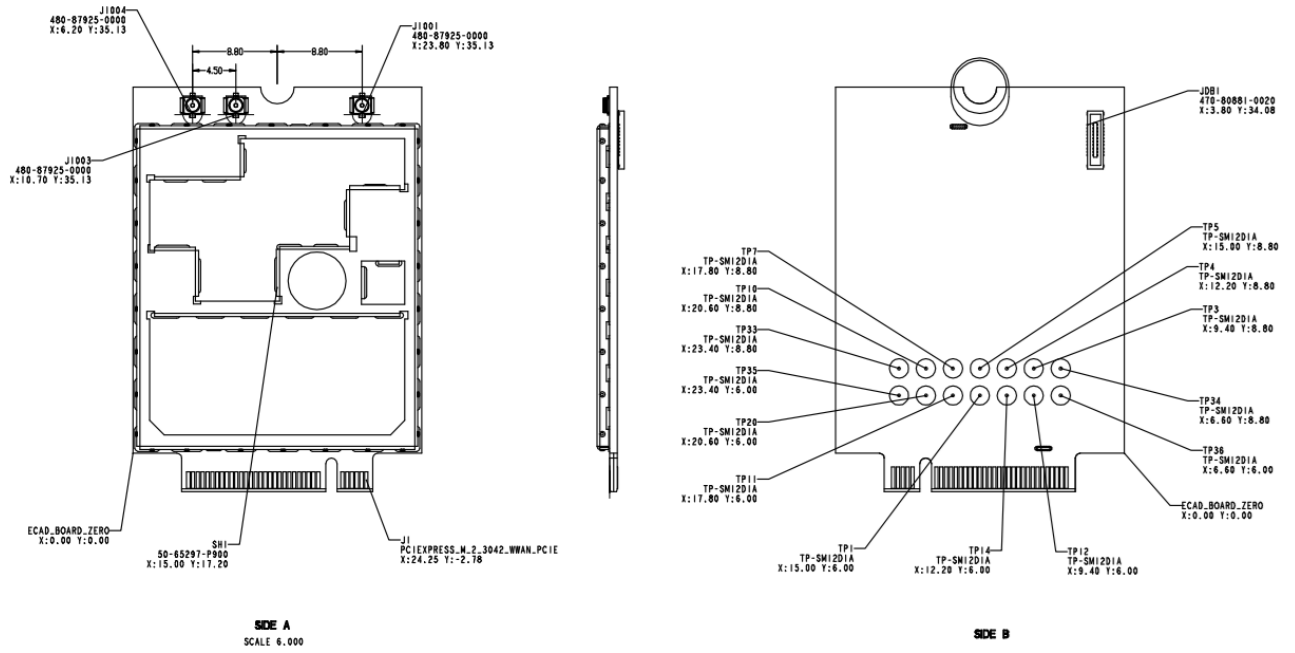
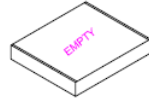


Figure 8-3 Module connectors locations

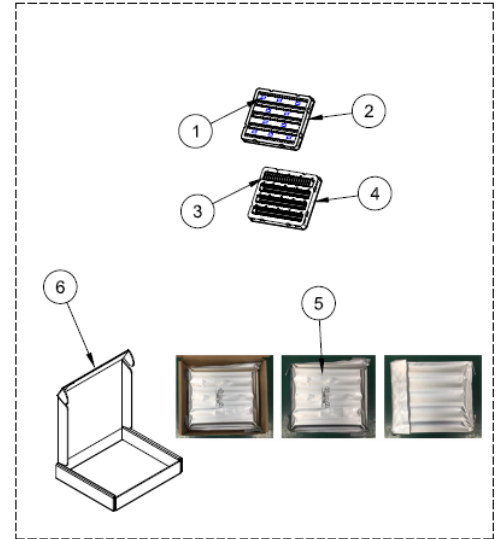
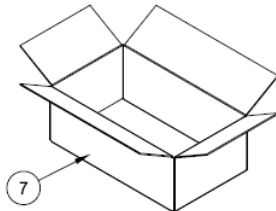
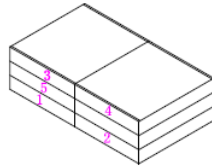
9. Package Information

NOTES:

1. Carton封箱時, 膠帶以H型封箱.
 Khi niêm phong thùng Carton, dán băng keo niêm phong theo hình chữ H.
2. 各零件內容之檢驗,請依各料號之材料承認書.
 Các kiểm tra nội dung từng linh kiện, dựa theo giấy chứng nhận nguyên vật liệu từng mã liệu (P/N).



未滿箱需放入空BOX, BOX上蓋, 蓋EMPTY章
 空BOX擺放優先順序, 按照下圖數字, 由1開始擺放空BOX
 Nếu hộp chưa đầy, bạn cần cho vào BOX trống, đẩy nắp lại và dán tem EMPTY.
 Thứ tự ưu tiên đặt BOX trống theo số trong hình bên dưới, bắt đầu từ số 1 cho đến khi đặt BOX trống



No	TITLE	QTY	No	TITLE	QTY
1	DESICCANT 3g	10/80	6	BOX	1/80
2	AES TRAY PLATE _TOP	1/80	7	CARTON(OD:543*328*218mm)	1/480
3	WNRMDQ-100	1			
4	AES TRAY PLATE _BOTTOM	7/80			
5	BAG-ESD ALUMINUM FOIL VACUUM	1/80			

Figure 9-1 Module package overview